Amendments to the Claims:

A listing of the entire set of pending claims (including amendments to the claims, if any) is submitted herewith per 37 CFR 1.121. This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Currently amended) A method of manufacturing an electronic device comprising thin-film circuit elements that include a diode ~~(D)~~ integrated with a crystalline thin-film transistor ~~(TFT)~~, the transistor having a channel area ~~(1)~~ in an active semiconductor film ~~(10)~~ that is more crystalline than an active semiconductor film ~~(40)~~ of the diode, ~~wherein the method includes~~ comprising:

~~(a)~~ a film formation step including forming on a circuit substrate ~~(100)~~ the crystalline active semiconductor film ~~(10)~~ of the transistor with a first process involving a first processing temperature;

~~(b)~~ a regions forming step including forming doped source and drain regions ~~(s1,s2, d1,d2)~~ of the transistor at ends of the channel area ~~(1)~~ with a second process involving a second processing temperature;

~~(c)~~ a film provisioning step including providing an interconnection film ~~(20)~~ between an electrode area ~~(s2, g1)~~ of the transistor and a diode area over which the diode ~~(D)~~ is to be formed, and providing an etch-stop film ~~(30)~~ on which the active semiconductor film ~~(40')~~ for the diode is to be deposited;

~~(d)~~ a film depositing step thereafter including depositing the active semiconductor film ~~(40')~~ for the diode over the interconnection film ~~(20)~~ and the etch-stop film ~~(30)~~ with a third process that involves a third processing temperature, ~~this stage (d)~~ the film depositing step being performed after ~~stages (a) and (b)~~ the film formation step and the regions forming step, and the first and second processing temperatures being higher than the third processing temperature; and

~~(e)~~ an etching step thereafter including etching away the active semiconductor film ~~(40')~~ for the diode from over the etch-stop film ~~(30)~~ to leave the

active semiconductor film ~~(40)~~ for the diode ~~(D)~~ over the interconnection film ~~(20)~~ in the diode area.

2. (Currently amended) ~~A method according to Claim~~ The method of claim 1, wherein the etch-stop film ~~(30)~~ is an insulating film ~~(2, 300~~ that extends over the interconnection film ~~(20)~~ and that has a window ~~(24)~~ at the diode area to permit contact between the interconnection film and the active semiconductor film of the diode.

3. (Currently amended) ~~A method according to Claim~~ The method of claim 2, wherein the diode has its active semiconductor film ~~(40)~~ forming an intrinsic region between P and N electrode regions ~~(41, 42)~~ of a vertical PIN diode structure, and wherein the interconnection film ~~(20)~~ comprises a doped region ~~(P+)~~ that is formed in ~~stage (b)~~ the regions forming step in a semiconductor film ~~(10)~~ together with the doped source and drain regions ~~(s1,s2, d1,d2)~~ of the transistor and a bottom one ~~(41)~~ of the P and N electrode regions of the PIN diode.

4. (Currently amended) ~~A method according to Claim~~ The method of claim 3, wherein regions of the crystalline active semiconductor film ~~(10)~~ provided in ~~stage (a)~~ the film formation step are doped in ~~stage (b)~~ the regions forming step to provide the source and drain regions of the transistor, the bottom one of the P and N electrode regions of the PIN diode, and the interconnection film therebetween.

5. (Currently amended) ~~A method according to Claim~~ The method of claim 3, wherein at least a portion of the interconnection film ~~(20)~~ is provided on a gate-dielectric film ~~(2)~~ on the crystalline active semiconductor film ~~(10)~~ to form a doped-semiconductor top gate electrode ~~(g1)~~ of the transistor which is thereby interconnected with the bottom one ~~(41)~~ of the P and N electrode regions of the PIN diode.

6. (Currently amended) ~~A method according to Claim~~ The method of claim 5, wherein the PIN diode is formed on the gate-dielectric film on the crystalline active semiconductor film of the transistor.

7. (Currently amended) ~~A method according to both Claim 4 and Claim 5~~ The method of claim 4, wherein the electronic device comprises first and second crystalline thin-film transistors ~~(TFT1, TFT2)~~ integrated with the PIN diode by means of the same interconnection film ~~(20)~~, and wherein the interconnection film ~~(20)~~ provides the bottom one ~~(41)~~ of the P and N electrode regions of the PIN diode, the top gate electrode ~~(g1)~~ of the first transistor, and/or the source and drain regions ~~(s2, d2)~~ of the second transistor.

8. (Currently amended) ~~A method according to Claim~~ The method of claim 1, wherein the interconnection film ~~(20, 461)~~ comprises metal which itself provides the etch-stop film ~~(30)~~, and the diode has a vertical PIN diode structure formed in its active semiconductor film as an intrinsic region between P and N electrode regions.

9. (Currently amended) ~~A method according to Claim~~ The method of claim 8, wherein at least a portion of the etch-stop interconnection film is provided on a gate-dielectric film ~~(2)~~ on the crystalline active semiconductor film to form a top gate electrode ~~(g1)~~ of the transistor which is thereby interconnected with a bottom one ~~(41)~~ of the P and N electrode regions of the PIN diode.

10. (Currently amended) ~~A method according to Claim~~ The method of claim 9, wherein the PIN diode is formed on the gate-dielectric film on the crystalline active semiconductor film of the transistor.

11. (Currently amended) ~~A method according to Claim~~ The method of claim 9 ~~or Claim 10~~, wherein the electronic device comprises first and second crystalline thin-film transistors ~~(TFT1, TFT2)~~ integrated with the PIN diode by means of the same

interconnection film ~~(20, 461)~~, and wherein the interconnection film connects the bottom one ~~(41)~~ of the P and N electrode regions of the PIN diode, the top gate electrode ~~(g1)~~ of the first transistor, and the source region ~~(s2)~~ of the second transistor.

12. (Currently amended) ~~A method according to Claim~~ The method of claim 7 ~~or Claim 11~~, wherein the electronic device comprises an active-matrix electroluminescent display with a light-emitting diode ~~(500, LED)~~ in each pixel, and wherein the light-emitting diode is driven via the first transistor ~~(TFT1)~~ as addressed via the second transistor ~~(TFT2)~~.

13. (Currently amended) ~~A method according to any one of the preceding Claims~~ The method of claim 1, wherein the crystalline semiconductor film ~~(10)~~ is subjected to a hydrogenation process that is performed after ~~stages (a)~~ the film formation step and ~~(b)~~ the regions forming step and before stage ~~(d)~~ film depositing step.

14. (Currently amended) ~~A method according to any one of the preceding Claims~~ The method of claim 1, wherein the crystalline semiconductor film ~~(10)~~ is formed in ~~stage (a)~~ the film formation step by crystallising a deposited semiconductor film using laser heating ~~(200)~~ of the film.

15. (Currently amended) ~~A method according to any one of the preceding Claims~~ The method of claim 1, wherein the doped source and drain regions are formed in ~~stage (b)~~ the regions forming step by an ion implant of dopant in the crystalline semiconductor film and by annealing ~~(201)~~ the implanted dopant.

16. (Currently amended) An electronic device comprising thin-film circuit elements that include a diode integrated with a crystalline thin-film transistor, wherein:

the transistor has at least one of its source, drain and gate electrodes formed as a doped region ~~(s2, g1)~~ of a crystalline semiconductor film ~~(10, 20)~~ that is more crystalline than an active semiconductor film ~~(40)~~ of the diode,

the doped region ~~(s2, g1)~~ of the crystalline semiconductor film extends from the transistor to provide a bottom electrode region ~~(41)~~ of the diode that is thereby interconnected with the said one ~~(s2, g1)~~ of the transistor source, drain and gate electrodes, and

the diode has its said active semiconductor film ~~(40)~~ on the crystalline semiconductor film ~~(10, 20)~~ at a window in an insulating etch-stop film ~~(2, 30)~~ that extends over the crystalline semiconductor film and over at least a portion of the crystalline thin-film transistor, the active semiconductor film ~~(40)~~ of the diode having a lateral extent that terminates on the insulating etch-stop film.

17. (Currently amended) ~~A device according to Claim~~ The device of claim16, wherein the diode has a vertical PIN structure having its said active semiconductor film as an amorphous intrinsic region ~~(40)~~ stacked between P and N electrode regions, and wherein the insulating etch-stop film ~~(2, 30)~~ extends between the bottom one ~~(41)~~ of the P and N electrode regions and the amorphous intrinsic region ~~(40)~~ at the lateral edge of the PIN diode.

18 ~~(Canceled)~~.

19. (New) The method of claim 5, wherein the electronic device comprises first and second crystalline thin-film transistors integrated with the PIN diode by means of the same interconnection film, and wherein the interconnection film provides the bottom one of the P and N electrode regions of the PIN diode, the top gate electrode of the first transistor, and/or the source and drain regions of the second transistor.

20. (New) The method of claim 10, wherein the electronic device comprises first and second crystalline thin-film transistors integrated with the PIN diode by means of the same interconnection film, and wherein the interconnection film connects the bottom one of the P and N electrode regions of the PIN diode, the top gate electrode of the first transistor, and the source region of the second transistor.

21. (New) The method of claim 11, wherein the electronic device comprises an active-matrix electroluminescent display with a light-emitting diode in each pixel, and wherein the light-emitting diode is driven via the first transistor as addressed via the second transistor.